REMARKS

Claims 1-20 are pending in the application. In response to the office action, applicants have amended claims 2, 3, 9, 10, and 12-20. Claims 1-20 remain pending for reconsideration.

The claims have been amended editorially for reasons not related to patentability. Namely, the claims have been amended to correct various editorial issues to and otherwise improve the claim language. No claim scope or equivalents are surrendered by way of the present amendments.

The title of the invention is objected to as not being descriptive. Applicants respectfully traverse this objection. The independent claims are directed to a multi-threading processor, a method for switching threads in a multi-threading processor, and set of instructions for switching threads, respectively. Applicants submit that the present title, Apparatus And Method For Switching Threads In Multi-Threading Processors, is more than sufficiently descriptive. If the Examiner has a proposed title in mind, applicants welcome such suggestion.

Claims 10, 13, 16, and 19 are objected to under 37 C.F.R. § 1.75 (c) for failing to further limit the subject matter of a previous claim. Applicants respectfully traverse this objection for the following reasons.

In a multi-threading processor, one of skill in the art would understand that the operation of switching a thread is a distinct operation from the operation of executing a thread, with the switching generally preceding the executing. Moreover, the office action fails to consider these claims as whole, with particular combinations of executed threads. Accordingly, the further recitations of the dependent claims 10, 13, 16, and 19 are properly dependent on their respective base claims, and the objection should be withdrawn.

Claims 10, 13, 16, and 19 were objected to under 35 U.S.C. § 112, second paragraph. Applicants respectfully traverse this rejection for the following reasons.

The office action objected to the phrase 'first inactive thread' being utilized in connection with an executing thread. Applicants submit that one of ordinary skill in the art would understand that such phrase merely identified the previously inactive thread being executed, and that the original claims were sufficiently definite. However, for business reasons not related to patentability, namely to expedite the prosecution, applicants have amended the claims to improve the claim language, now reciting third and fourth threads. Applicants submit that amended claims 10, 13, 16, and 19 are in proper form.

Claims 1-4 and 9-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by the article Simultaneous Multithreading: A Platform for Next-Generation Processors (hereinafter Eggers). Claims 5-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eggers. Applicants respectfully traverse these rejections for the following reasons.

The analysis set forth in the office action falls short for several reasons. In order to anticipate, the reference must identically disclose each and every claim recitation. Claim 1 recites a first instruction fetch unit and a second instruction fetch unit. Eggers discloses only a single instruction fetch unit that separately fetches two instructions. The office action relies on Page 14, left column of Eggers for allegedly describing that the single fetch unit "partitions itself among the threads." However, applicants are unable to identify any teaching of such "partitioning." If the rejection is maintained, applicants respectfully request clarification of the precise portion of Eggers which allegedly describes such partitioning, justifying the Examiner's reliance on a single fetch unit for anticipating the recited first and second instruction fetch units.

Claim 1 further recites a multi-thread scheduler unit coupled to said first instruction fetch unit and said second instruction fetch unit. The office action relies on page 13, left hand column, particularly the description of Fig. 1c, for allegedly identically

disclosing this claim recitation. However, the cited portion merely generally describes how one form of SMT might work, and does not describe any particular structure. Specifically, the cited portion does not describe a scheduler unit coupled to first and second instruction fetch units. In fact, the entire Eggers reference is devoid of any block diagram or other structural description of a fully functional SMT processor. The reference only merely describes different SMT capabilities that are proposed to improve multithreading performance. If the rejection is maintained, applicants respectfully request clarification of the precise portion of Eggers which allegedly describes a scheduler unit coupled to first and second instruction fetch units.

Claim 1 further recites an execution unit coupled to said scheduler unit, wherein said execution unit is to execute a first active thread and a second active thread. The office action apparently relies on the entirety of pages 13 and 14 for allegedly identically describing this claim recitation. Applicants first note that such bulk citation fails to comply with 37 C.F.R. § 104(c)(2) because the office action does not sufficiently designate the particular part(s) of the reference(s) relied upon for disclosing each claim recitation. Applicants have reviewed pages 13 and 14 and cannot identify any mention of an execution unit or how such unit might be interconnected with other units. Applicants are not required to guess as to how the reference is being applied to the claim. If the rejection is maintained, a new non-final action is respectfully requested with a sufficiently detailed explanation of the Examiner's position, so that a full and fair response may be made.

In any event, applicants again note that Eggers does not appear to describe any particular structure for the SMT processor alluded to therein. Rather, Eggers appears to be an academic paper describing proposals for processor designers to further investigate SMT techniques to improve multithreading processors.

Claim 1 further recites a register file coupled to said execution unit, wherein said register file is to switch one of said first active thread and said second active thread with a first inactive thread. The office action relies on pages 14-15, particularly the section entitled "Register file and pipeline," for allegedly identically disclosing this claim recitation. Applicants are unable to identify any description in the cited portion that discloses a register file coupled to an execution unit or that the registers described in the

"Register file" section are used to switch either a first or second active thread with an inactive thread. The office action goes on to identify actions described in Eggers as occurring at the fetch unit, not the register file. Namely, that the fetch unit may select two of an available eight threads for decoding. Applicants do not understand the Examiner's analysis with respect to how the fetching of instructions by Eggers' fetch unit teaches or suggest anything whatsoever in connection with the operation of Eggers' register file. The office action appears to be improperly conflating these two distinct components of Eggers in order to read on the claims. In any event, selecting among available threads for execution in an SMT is different from and does not teach or suggest the recited switching of an active thread with an inactive thread.

By way if background, some embodiments of the present invention may relate to a multithreading processor which exhibits both simultaneous multithreading (SMT) capability and switch on event multithreading (SoEMT) capability. In contrast, Eggers describes only multithreading processors having either SMT capability or SoEMT capability. Accordingly, Eggers cannot possibly anticipate the present claims or render the present claims unpatentable. In fact, Eggers teach away from such a combination of functionality because Eggers clearly suggests using SMT capabilities instead of SoEMT capabilities. According to Eggers, "SMT was able to get higher instruction throughput and greater program speedups than the fine-grained multithreading processor" (i.e. an SoEMT processor). See Eggers, page 17, section entitled "SMT vs. fine-grained multithreading."

For example, claim 1 recites an execution unit to execute a first active thread and a second active thread (e.g. SMT capability), and a register file to switch one of said first active thread and said second active thread with a first inactive thread (e.g. SoEMT capability). Among other things, Eggers fails to teach or suggest a multithreading processor with both these capabilities, as recited in claim 1.

For the foregoing reasons, in particular because Eggers fails to teach or suggest the various recitation noted above in claim 1, claim 1 is not anticipated by and is

patentable over Eggers. Claims 2-8 depend either directly or indirectly from claim 1 and are likewise patentable.

With respect to claim 2, applicants note that Eggers does not describe how the "hardware contexts for eight threads" are otherwise interconnected. In any event, they do not appear to be coupled to the disclosed "register file." Accordingly, claim 2 is separately patentable over Eggers.

With respect to claim 4, applicants note that the office action relies on Page 14, first paragraph, which does not appear to mention any decoders. The only mention of decoding applicants can identify is in the paragraph spanning the left and right columns on Page 14, which describes that Eggers single fetch unit selects subset of instructions from two threads for decoding. Accordingly, Eggers does not teach or suggest first and second decode units. Accordingly, claim 4 is separately patentable over Eggers.

With respect to claim 5, applicants again note that Eggers does not describe any particular structure for the SMT processor proposed therein. Moreover, Eggers at most describes a single fetch unit which can fetch two or more instructions in a given cycle for decoding by a single decode unit. This is different from and does not teach or suggest the structure of multiple (e.g. first through fourth) instruction fetch units as recited in claim 5. Accordingly, claim 5 is separately patentable over Eggers.

With respect to claim 6, applicants note that the register file mentioned in Eggers appears to have a different structure and function as compared to the recited four way register file. Merely changing the size of the register file described in Eggers still does not read on the recited four way register file. Accordingly, claim 6 is separately patentable over Eggers.

With respect to claim 7, the office action again appears to improperly conflate the functions of Eggers' fetch unit with Eggers' register file. The Examiner should unambiguously identify whether the rejection relies on Eggers' fetch unit or Eggers'

register file for the recited switching, so that a full and fair response may be made. In the absence of such unambiguous analysis, the office action is in error as to what is taught or suggested by Eggers and fails to establish a prima facie case of obviousness. Accordingly, claim 7 is separately patentable over Eggers.

With respect to claim 8, applicants again note that Eggers does not describe any particular structure for the SMT processor proposed therein. Moreover, Eggers at most describes a single fetch unit which can fetch two or more instructions in a given cycle for decoding by a single decode unit. This is different from and does not teach or suggest the structure of multiple (e.g. first through fourth) decode units as recited in claim 8. Accordingly, claim 8 is separately patentable over Eggers.

With respect to independent claims 9 and 15, the office action misconstrues the Eggers reference. Claims 9 and 15 each recite switching a first active thread with a third thread, if the third thread is ready to execute. The office action relies on the description of the how Eggers' fetch unit operates for allegedly identically disclosing this claim recitation. However, the operation of the fetch unit in Eggers does not have anything to do with active thread switching. As acknowledged by the Examiner in the office action, active threads are those threads which are executing. Eggers' fetch unit selects among various inactive instructions for execution. However, at the time of the instructions fetch, such instructions would not be considered active threads by those skilled in the art. Rather, the selected instructions become active at the time of execution.

Accordingly, the office action is in error by relying upon operations occurring at Eggers' fetch unit to read upon either of the detecting or switching recitations, which relate to an active thread. As noted above, the cited portion of Eggers describes only a multithreading processor having SMT capability, not SoEMT capability. Accordingly, the only action Eggers teaches or suggests in connection with active threads during an execution cycle is the simultaneous execution of the active threads. When a stalling event occurs, the active thread becomes inactive and stops executing. The cited portion of Eggers, namely page 14, left hand column, describes that during the next instruction

fetch cycle, a new instruction may be fetched to replace the now inactive instruction, but Eggers does not teach or suggest switching an active thread with a new thread after detecting a stalling event in the active thread.

Because, among other things, Eggers fails to teach or suggest the recited switching said first active thread with a third thread, if the third thread is ready to execute, claims 9 and 15 are not anticipated by and are patentable over Eggers. Claims 10-14 depend from claim 9 and are likewise patentable. Claims 16-20 depend from claim 15 and are likewise patentable.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

October 11, 2004
Date

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I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office at (703) 872-9306 on October 11, 2004.

Paul E. Steiner **Date: October 11, 2004**